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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,200	03/08/2001	Kenji Shimazaki	61282-011	4112

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,200	SHIMAZAKI ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-37 are pending.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 03/08/2001 and 5/19/06 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS' as to the merits.

The information disclosure statement filed 10/10/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The following is a non-exhaustive list of 35 U.S.C. 112 second paragraph violations in the claims:

Claim 1:

- The preamble cites 'a method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation'. However, the claim is directed to performing FFT's on current change information, and the Examiner is unclear regarding how and where the EMI of the LSI is simulated.
- The meaning of the term 'performing modeling' is unclear because the claim does not specify what is being modeled, and this renders the claim indefinite.
- The meaning of the term 'current change information' is unclear and this renders the claim indefinite.

Claim 2:

- The Examiner is unclear regarding what is meant by 'allocating different discrete FFT analysis frequency widths to the specified frequency range and to a frequency range other than the specified frequency range'.

- The meaning of the term 'performing modeling' is unclear because the claim does not specify what is being modeled, and this renders the claim indefinite.

Claim 3:

- The meaning of the term 'current frequency component' is unclear and this renders the claim indefinite.

Claim 4:

- The meaning of the term 'current frequency component' is unclear and this renders the claim indefinite.
- The Examiner is unclear regarding what object is being analyzed in the method.

Claim 5:

- The meaning of the term 'a current frequency component storage step' is unclear and this renders the claim indefinite.
- The meaning of the term 'storing in the current frequency component storage means' is unclear and this renders the claim indefinite.
- The meaning of the term 'a predetermined threshold' is unclear and this renders the claim indefinite.

Claim 6:

- The meaning of the term 'a current frequency component storage step' is unclear and this renders the claim indefinite.

- The meaning of the term 'storing in the current frequency component storage means' is unclear and this renders the claim indefinite.
- The meaning of the term 'order of magnitude' is unclear and this renders the claim indefinite.

Claim 7:

- The meaning of the term 'a current frequency component' is unclear and this renders the claim indefinite.

Claim 8:

- The meaning of the term 'a current frequency component' is unclear and this renders the claim indefinite.

Claim 9:

- The meaning of the term 'a current frequency component' is unclear and this renders the claim indefinite.

Claims 10 & 11:

- The meaning of the term 'a current frequency component' is unclear and this renders the claim indefinite.
- The meaning of the term 'logic change numbers' is unclear and this renders the claim indefinite.
- The meaning of the term 'a predetermined threshold' is unclear and this renders the claim indefinite.

Claim 12:

- The meaning of the term 'a current frequency component' is unclear and this renders the claim indefinite.
- The meaning of the term 'logic change numbers' is unclear and this renders the claim indefinite.

Claims 13 & 14:

- The Examiner is unclear regarding what 'identifying an instance name which mainly causes noise in an associated frequency component with large noise' means.
- The meaning of the term 'large noise' is unclear and this renders the claim indefinite.

Claim 15:

- The Examiner is unclear regarding what is meant by 'grouping instances according to flag information written in library or for grouping them into instance groups'.
- The meaning of the terms 'instance', 'flag information', and 'library' are unclear and this renders the claim indefinite.

Claim 16:

- The meaning of the term 'instance' is unclear and this renders the claim indefinite.

Claim 17:

- The meaning of the term 'instance' is unclear and this renders the claim indefinite.

- The meaning of the term 'status changes' is unclear and this renders the claim indefinite.

Claim 18:

- The meaning of the term 'instance grouping information' is unclear and this renders the claim indefinite.
- The meaning of the term 'large noise' is unclear and this renders the claim indefinite.
- The Examiner is unclear regarding what is meant by 'an instance name which mainly causes noise in an associated frequency component with large noise and then reporting information on noise level'.

Claim 20:

- The preamble cites 'a method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation'. However, the claim is directed to correcting a model of a current waveform using a correction coefficient, and the Examiner is unclear regarding how and where the EMI of the LSI is simulated.
- The meaning of the term 'correction step' is unclear and this regards the claim indefinite.
- The Examiner is unclear regarding how a resistance and capacitance (calculated from just the power supply circuit of the chip) can be used to calculate the equivalent resistance and capacitance of the entire chip.

- The Examiner is unclear regarding what 'an event-based model of an estimated current waveform obtained in advance as an ideal power supply' means.

Claim 21:

- The Examiner is unclear regarding how a resistance and capacitance (calculated from just the power supply circuit of the chip) can be used to calculate the equivalent resistance and capacitance of the entire chip.
- The Examiner is unclear regarding what 'calculating the correction coefficient by performing processing according to a table prepared in advance' means.

Claim 22:

- The Examiner is unclear regarding how a resistance and capacitance (calculated from just the power supply circuit of the chip) can be used to calculate the equivalent resistance and capacitance of the entire chip.
- The Examiner is unclear regarding what 'calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance' means.
- The meaning of the term 'a mathematical expression prepared in advance' is unclear and this regards the claim indefinite.

Claim 23:

- The Examiner is unclear regarding what 'correcting a base of the event-based model' means.

Claim 24:

- The Examiner is unclear regarding what 'correcting an area of the event-based model of the estimated current waveform' means.

Claim 25:

- The Examiner is unclear regarding how shape information can be used to calculate the equivalent information of the chip.
- The meaning of the term 'shape information' is unclear and this regards the claim indefinite.
- The Examiner is unclear regarding what 'calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance' means.
- The meaning of the term 'high speed' is unclear and this regards the claim indefinite.

Claim 26:

- The preamble cites 'a method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation'. However, the claim is directed to estimating an equivalent resistance and capacitance of the power circuit, calculating a correction coefficient, and then correcting a model of the current waveform, and the Examiner is unclear regarding how and where the EMI of the LSI is simulated.
- The meaning of the term 'correction coefficient' is unclear and this regards the claim indefinite.

- The meaning of the term 'an event-based model of an estimated current waveform' is unclear and this regards the claim indefinite.

Claim 27:

- The meaning of the term 'an area of the chip' is unclear and this regards the claim indefinite.

Claim 28:

- The meaning of the term 'technology information' is unclear and this regards the claim indefinite.

Claim 29:

- The meaning of the terms 'chip shape' and 'power supply pad position' are unclear and this regards the claim indefinite.

Claim 30:

- The Examiner is unclear regarding how the number of power supply pads is used to calculate equivalent resistances and capacitances.

Claim 30:

The Examiner is unclear regarding how the width of the power supply pads is used to calculate equivalent resistances and capacitances.

Claim 32:

- The meaning of the term 'a capacitance generation area' is unclear and this regards the claim indefinite.

Claims 33 & 34:

- The meaning of the term 'module' is unclear and this regards the claim indefinite.
- The meaning of the term 'correction coefficient' is unclear and this regards the claim indefinite.

Claim 35:

- The Examiner is unclear regarding how a resistance and capacitance (calculated from just the power supply circuit of the chip) can be used to calculate the equivalent resistance and capacitance of the entire chip.
- The Examiner is unclear regarding what 'calculating the correction coefficient by using a table or mathematical expression prepared in advance' means.

Claim 37:

- The Examiner is unclear regarding what 'the current waveform correction step corrects the current waveform obtained as an ideal power supply' means.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 20, and 26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product.

As per **claim 1**, the last step of the claim performs FFTs' on the current change information. This is neither a tangible nor useful result because the results from the FFTs are not stored or used for any other purpose (i.e. the claim language does not disclose how the results from the FFTs' can be used to simulate EMI).

As per **claims 20 and 26**, the last steps of the claims correct an already existent event-based model of an estimated current waveform. This is not a tangible output. Also, this is not a useful output because the claim language does not disclose how the corrected model can be used to analyze the EMI of LSI.

Claims 1-37 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by a specific and substantial asserted utility, or a well established utility.

By reading the claims, a skilled artisan would not be able to understand and produce the invention. The claim language is vague. The specification is lengthy and unclear, and it would be unclear to a skilled artisan reviewing the specification where the invention is enabled.

Claims 1-37 also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

Claim Interpretation

Numerous 112 rejections have been applied against the claims. MPEP section 2143.03 addresses the issue of applying prior art against such claims:

> A claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. 112, second paragraph (see MPEP § 706.03(d)) and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. Ex parte Ionescu, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984) (Claims on appeal were rejected on indefiniteness grounds only; the rejection was reversed and the case remanded to the examiner for consideration of pertinent prior art.). Compare In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious) and In re Steele, 305 F.2d 859,134 USPQ 292 (CCPA 1962) (it is improper to rely on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. 103 on these assumptions).

See also section 2173.06 (Prior Art Rejection of Claim Rejected as Indefinite):

> All words in a claim must be considered in judging the patentability of a claim against the prior art. In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970).

The fact that terms may be indefinite does not make the claim obvious over the prior art. When the terms of a claim are considered to be indefinite, at least two approaches to the examination of an indefinite claim relative to the prior art are possible. First, where the degree of uncertainty is not great, and where the claim is subject to more than one interpretation and at least one interpretation would render the claim unpatentable over the prior art, an appropriate course of action would be for the examiner to enter two rejections: (A) a rejection based on indefiniteness under 35 U.S.C. 112, second paragraph; and (B) a rejection over the prior art based on the interpretation of the claims which renders the prior art applicable. See, e.g., Ex parte Ionescu, 222 USPQ 537 (Bd. App. 1984). When making a rejection over prior art in these circumstances, it is important for the examiner to point out how the claim is being interpreted. Second, where there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of a claim, it would not be proper to reject such a claim on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection under 35 U.S.C. 103 should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. The first approach is recommended from an examination standpoint because it avoids piecemeal examination in the event that the examiner's 35 U.S.C. 112, second paragraph rejection is not affirmed, and may give applicant a better appreciation for relevant prior art if the claims are redrafted to avoid the 35 U.S.C. 112, second paragraph rejection.

There is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of claims 1-37, and thus it would not be proper to reject such a claim on the basis of prior art. However, in the interests of compact prosecution, such an interpretation will be nonetheless provided. **The subsequent prior art rejections are asserted in view of the following claim analysis.**

The *Examiner interprets claim 1* to be directed to modeling an LSI circuit, gathering current information from the model, and performing FFT operations on the current information by first breaking up the signal into different frequency ranges (or bins), and then computing the FFT for each bin.

The *Examiner interprets the first step of claim 2* to be directed to changing the width of the FFT frequency bins. The 112 2nd rejection applied to the second step of the claim render it indefinite.

The *Examiner interprets claim 3* to be directed to deriving a current waveform of the model.

The *Examiner interprets the first step of claim 20* to be directed to calculating equivalent resistances and capacitances of the power model of the network. The 112 2nd rejection made to the second step of the claim renders it indefinite.

The *Examiner interprets the first step of claim 26* to be directed to calculating equivalent resistances and capacitances of the power model of the network. The *Examiner interprets the third step of claim 26* to be directed to producing an event-based model of an estimated current

waveform obtained in advance as an ideal power supply. The 112 2nd rejection made to the second step of the claim renders it indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1-3, 20, and 26 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Hayashi et al ('EMI-Noise Analysis under ASIC Design Environment')**, herein referred to as Hayashi.

As per **claims 1-3**, Hayashi discloses performing EMI-noise analysis in an ASIC design environment (Abstract). After a netlist for the *model* is generated, switching current waveforms are obtained. Logic simulation is then performed using the Verilog netlist and test vectors. Current waveforms are then obtained by superposing current waveforms in the Cell Current Waveform Library according to event data. Power network data is then extracted, and *FFTs are performed on current waveforms*.

Hayashi does not explicitly disclose performing the FFTs by first breaking the signal into frequency bins. However, a skilled artisan would obviously know that to perform FFTs on the current signal, the signal should be divided into frequency bins, and FFTs should then be performed on each frequency bin. The skilled artisan would also know that the widths of the FFTs can be altered through the use of any well-known windowing function.

As per **claim 20**, Hayashi discloses calculating the *equivalent resistance and capacitance* of the power model of the network (section 2.1).

As per **claim 26,** Hayashi discloses calculating the *equivalent resistance and capacitance* of the power model of the network (section 2.1). Hayashi further discloses the switching current consumed is simulated through the use of an *ideal power supply voltage* (section 2 paragraph 1).

waveform obtained in advance as an ideal power supply. The 112 2nd rejection made to the second step of the claim renders it indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER